



3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

MAX3362

General Description

The MAX3362 low-power, high-speed transceiver for RS-485/RS-422 communication operates from a single +3.3V power supply. The device contains one differential transceiver consisting of a line driver and receiver. The transceiver operates at data rates up to 20Mbps, with an output skew of less than 6ns. Driver and receiver propagation delays are guaranteed below 50ns. This fast switching and low skew make the MAX3362 ideal for multidrop clock/data distribution applications.

The output level is guaranteed at +1.5V with a standard 54Ω load, compliant with RS-485 specifications. The transceiver draws 1.7mA supply current when unloaded or fully loaded with the drivers disabled. Additionally, the MAX3362 has a low-power shutdown mode, reducing the supply current to 1μA.

The MAX3362 has a 1/8-unit-load receiver input impedance, allowing up to 256 transceivers on the bus. The MAX3362 is designed for half-duplex communication. The device has a hot-swap feature that eliminates false transitions on the data cable during circuit initialization. The drivers are short-circuit current limited, and a thermal shutdown circuit protects against excessive power dissipation.

The MAX3362 is available in an 8-pin SOT package and specified over industrial and automotive temperature ranges.

Applications

Clock/Data Distribution
Telecom Equipment
Security Equipment
Point-of-Sale Equipment
Industrial Controls

Pin Configuration and Functional Diagram appear at end of data sheet.

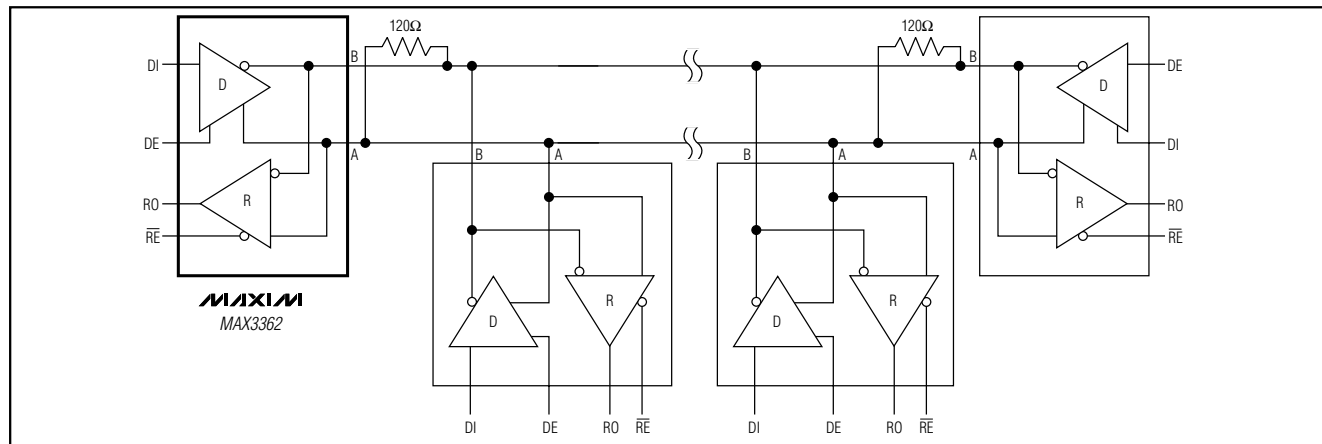
Features

- ◆ Space-Saving 8-Pin SOT Package
- ◆ Guaranteed 20Mbps Data Rate
- ◆ Operates from a Single +3.3V Supply
- ◆ 6ns (max) Transmitter and Receiver Skew
- ◆ Hot-Swap Feature
- ◆ Interoperable with +5V Logic
- ◆ Allows up to 256 Transceivers on the Bus
- ◆ 1μA Low-Power Shutdown Mode
- ◆ 1.7mA Operating Supply Current
- ◆ -7V to +12V Common-Mode Range
- ◆ Current Limiting and Thermal Shutdown
- ◆ Half-Duplex Operation
- ◆ Automotive Temperature Range Variants

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | TOP MARK |
|------------|-----------------|-------------|----------|
| MAX3362EKA | -40°C to +85°C | 8 SOT23 | AAJL |
| MAX3362AKA | -40°C to +125°C | 8 SOT23 | AALL |

Typical Operating Circuit



3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

ABSOLUTE MAXIMUM RATINGS

All voltages with respect to GND.

| | |
|--|------------------------------|
| V_{CC} , \overline{RE} , DE, DI | -0.3V to +6V |
| Receiver Input Voltages, Driver Output Voltages (A, B) | -8V to +13V |
| Receiver Input Current, Driver Output Current (A, B) | 250mA |
| $I_{VA} - I_{VB}$ | +8V |
| Receiver Output Voltage (RO) | -0.3V to ($V_{CC} + 0.3V$) |

Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

8-Pin SOT (derate 9.7mW/ $^\circ\text{C}$ above $+70^\circ\text{C}$) 777mW

Operating Temperature Range

MAX3362E -40 $^\circ\text{C}$ to +85 $^\circ\text{C}$

MAX3362A -40 $^\circ\text{C}$ to +125 $^\circ\text{C}$

Storage Temperature Range -65 $^\circ\text{C}$ to +150 $^\circ\text{C}$

Junction Temperature +150 $^\circ\text{C}$

Lead Temperature (soldering, 10s) +300 $^\circ\text{C}$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC} = +3.3V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ\text{C}$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------|---|------|-----|---------|---------------|
| DRIVER | | | | | | |
| Differential Driver Output | V_{OD} | Figure 1, $R_L = 100\Omega$ (RS-422) (extended temperature range) | 2.0 | | | V |
| | | Figure 1, $R_L = 100\Omega$ (automotive temperature range) | 1.5 | | | |
| | | Figure 1, $R_L = 54\Omega$ (RS-485) (extended temperature range) | 1.5 | | | |
| Change in Magnitude of Differential Output Voltage | ΔV_{OD} | Figure 1, $R_L = 54\Omega$ or 100Ω (Note 3) | | | 0.2 | V |
| Driver Common-Mode Output Voltage | V_{OC} | Figure 1, $R_L = 54\Omega$ or 100Ω | | | 3 | V |
| Change In Magnitude of Common-Mode Voltage | ΔV_{OC} | Figure 1, $R_L = 54\Omega$ or 100Ω (Note 3) | | | 0.2 | V |
| Input High Voltage | V_{IH} | DE, DI, \overline{RE} | 2.0 | | | V |
| Input Low Voltage | V_{IL} | DE, DI, \overline{RE} | | | 0.8 | V |
| Input Hysteresis | V_{HYS} | DE, DI, \overline{RE} | | 50 | | mV |
| Input Current (DE, DI, \overline{RE}) | I_{IN} | $0 \leq V_{IN} \leq 5V$ | | | ± 1 | μA |
| Driver Short-Circuit Output Current | I_{OSD} | $0 \leq V_{OUT} \leq 12V$ (Note 4) | | | +250 | mA |
| | | $-7V \leq V_{OUT} \leq V_{CC}$ (Note 4) | -250 | | | |
| Driver Short-Circuit Foldback Output Current | I_{OSDF} | $(V_{CC} - 1V) \leq V_{OUT} \leq 12V$ (Note 4) | +25 | | | mA |
| | | $-7V \leq V_{OUT} \leq 1V$ (Note 4) | | | -25 | |

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

MAX3362

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +3.3V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Notes 1, 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-----------------|---------------------------------------|-----------------|-------|-----------|------------|
| Thermal Shutdown Threshold | V_{TS} | | | 150 | | $^\circ C$ |
| Thermal Shutdown Hysteresis | V_{TSH} | | | 10 | | $^\circ C$ |
| RECEIVER | | | | | | |
| Receiver Differential Threshold Voltage | V_{TH} | $-7V \leq V_{CM} \leq 12V$ | -200 | 0 | +200 | mV |
| Receiver Input Hysteresis | ΔV_{TH} | $V_A + V_B = 0$ | | 25 | | mV |
| Receiver Output High Voltage | V_{OH} | $I_O = -1mA$, $V_A - V_B = V_{TH}$ | $V_{CC} - 0.4$ | | | V |
| Receiver Output Low Voltage | V_{OL} | $I_O = 1mA$, $V_A - V_B = -V_{TH}$ | | | 0.4 | V |
| Three-State Output Current at Receiver | I_{OZR} | $0 \leq V_O \leq V_{CC}$ | | | ± 1 | μA |
| Receiver Input Resistance | R_{IN} | $V_{CM} = 12V$ | 96 | | | $k\Omega$ |
| Receiver Input Current | I_{IN} | DE = GND, $V_{CC} = GND$ or 3.465V | $V_{IN} = +12V$ | | 125 | μA |
| | | | $V_{IN} = -7V$ | -100 | | |
| Receiver Output Short-Circuit Current | I_{OSR} | $0 \leq V_{RO} \leq V_{CC}$ | | | ± 150 | mA |
| POWER SUPPLY | | | | | | |
| Supply Voltage | V_{CC} | | 3.135 | 3.300 | 3.465 | V |
| Supply Current in Normal Operation (Static Condition) | I_Q | No load, DI = V_{CC} or GND | | 1.7 | 3 | mA |
| Supply Current in Shutdown Mode | I_{SHDN} | DE = GND, $\overline{RE} = V_{CC}$ | | 1 | 10 | μA |

SWITCHING CHARACTERISTICS (MAX3362E_ _ only)

($V_{CC} = +3.3V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-------------|--|-----|-----|------|-------|
| Driver Propagation Delay | t_{PDLH} | Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$ | | | 50 | ns |
| | t_{PDHL} | | | | 50 | |
| Driver Differential Output Rise or Fall Time | t_{DR} | Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$ | | | 12.5 | ns |
| | t_{DF} | | | | 12.5 | |
| Driver Output Skew | t_{DSKEW} | Figures 2 and 3, $R_L = 54\Omega$, $C_L = 50pF$ $t_{DSKEW} = t_{PDLH} - t_{PDHL} $ | | | 6 | ns |
| Maximum Data Rate | f_{MAX} | | 20 | | | Mbps |
| Driver Enable to Output Low | t_{PDZL} | Figure 4, $R_L = 500\Omega$, $C_L = 50pF$ | | | 100 | ns |
| Driver Disable Time from Low | t_{PDLZ} | Figure 4, $R_L = 500\Omega$, $C_L = 50pF$ | | | 100 | ns |
| Driver Disable Time from High | t_{PDHZ} | Figure 5, $R_L = 500\Omega$, $C_L = 50pF$ | | | 100 | ns |

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SWITCHING CHARACTERISTICS (MAX3362E__ only) (continued)

($V_{CC} = +3.3V \pm 5\%$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------------|---|-----|------|------|-------|
| Driver Enable to Output High | t _{PDZH} | Figure 5, $R_L = 500\Omega$, $C_L = 50pF$ | | | 100 | ns |
| Receiver Propagation Delay | t _{PRLH} | Figure 6, $C_L = 15pF$ | | | 50 | ns |
| | t _{PRHL} | | | | 50 | |
| Receiver Output Skew | t _{RSKEW} | Figure 6, $C_L = 15pF$ $t_{RSKEW} = t_{PRLH} - t_{PRHL} $ | | | 6 | ns |
| Receiver Enable to Output Low | t _{PRZL} | Figure 7, $R_L = 1k\Omega$, $C_L = 15pF$ | | | 100 | ns |
| Receiver Enable to Output High | t _{PRZH} | Figure 7, $R_L = 1k\Omega$, $C_L = 15pF$ | | | 100 | ns |
| Receiver Disable Time from Low | t _{PRLZ} | Figure 7, $R_L = 1k\Omega$, $C_L = 15pF$ | | | 100 | ns |
| Receiver Disable Time from High | t _{PRHZ} | Figure 7, $R_L = 1k\Omega$, $C_L = 15pF$ | | | 100 | ns |
| Time to Shutdown | t _{SD} | (Note 5) | 50 | | 600 | ns |
| Driver Enable from Output High to Shutdown | t _{PDHS} | | 50 | | 600 | ns |
| Driver Enable from Output Low to Shutdown | t _{PDLS} | | 50 | | 600 | ns |
| Receiver Enable from Output High to Shutdown | t _{PRHS} | | 50 | | 600 | ns |
| Receiver Enable from Output Low to Shutdown | t _{PRLS} | | 50 | | 600 | ns |
| Time to Normal Operation | t _{NO} | (Note 6) | | 1500 | 3000 | ns |
| Driver Enable from Shutdown to Output High | t _{PDSH} | Figure 5 $R_L = 500\Omega$, $C_L = 50pF$ | | 1500 | 3000 | ns |
| Driver Enable from Shutdown to Output Low | t _{PDSL} | Figure 4 $R_L = 500\Omega$, $C_L = 50pF$ | | 1500 | 3000 | ns |
| Receiver Enable from Shutdown to Output High | t _{PRSH} | Figure 7 $R_L = 1k\Omega$, $C_L = 15pF$ | | 1500 | 3000 | ns |
| Receiver Enable from Shutdown to Output Low | t _{PRSL} | Figure 7 $R_L = 1k\Omega$, $C_L = 15pF$ | | 1500 | 3000 | ns |

Note 1: Devices production tested at $+25^\circ C$. Over-temperature limits are guaranteed by design.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referenced to device ground, unless otherwise noted.

Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC} , respectively, when the DI input changes state.

Note 4: The short-circuit output current applies to peak current just prior to foldback-current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Note 5: Shutdown is enabled by bringing \overline{RE} high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

Note 6: Transition time from shutdown mode to normal operation.

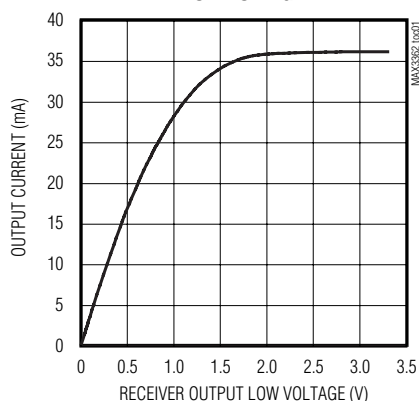
3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

Typical Operating Characteristics

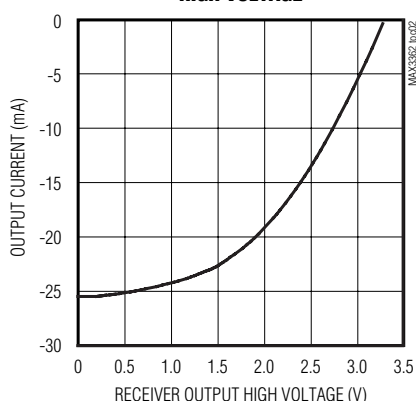
($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX3362

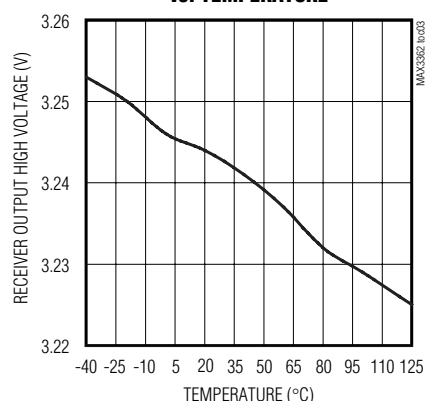
OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



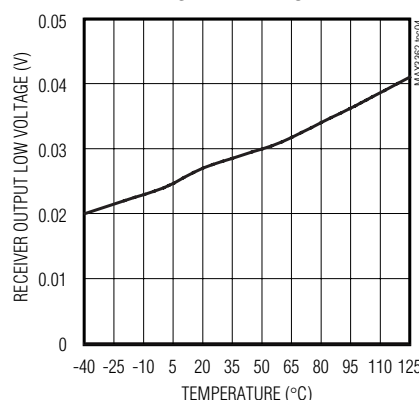
OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



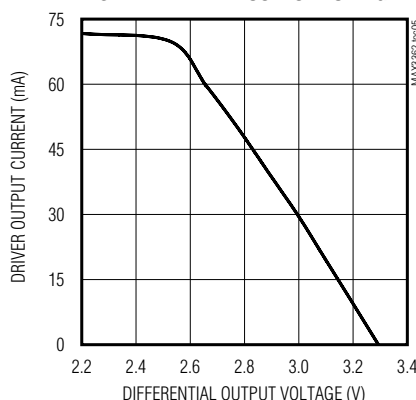
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



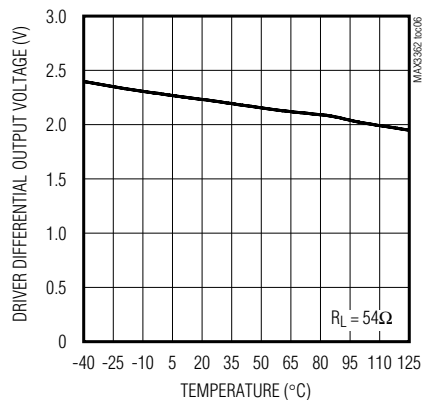
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



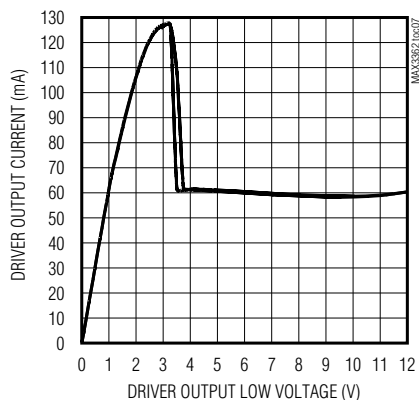
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



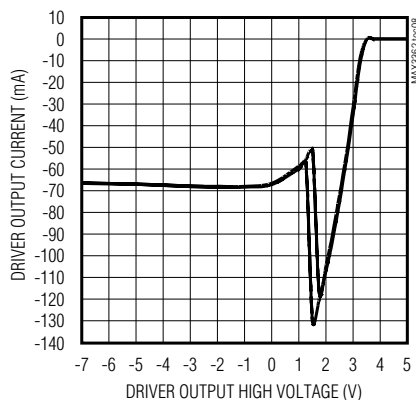
DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE



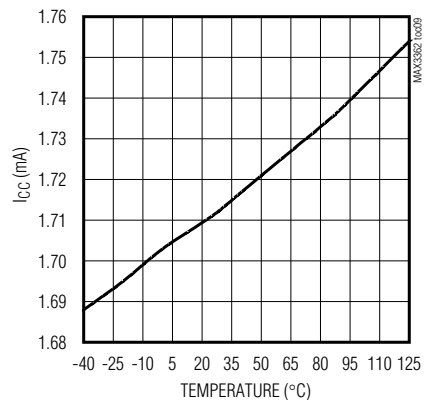
DRIVER OUTPUT CURRENT vs. DRIVER OUTPUT LOW VOLTAGE



DRIVER OUTPUT CURRENT vs. DRIVER OUTPUT HIGH VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

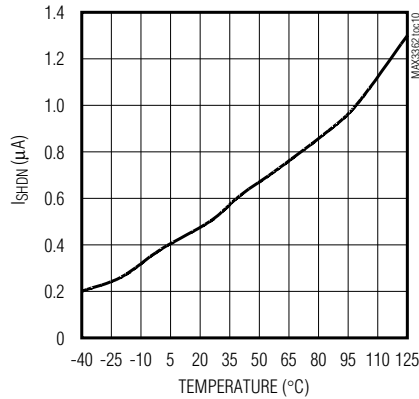


3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

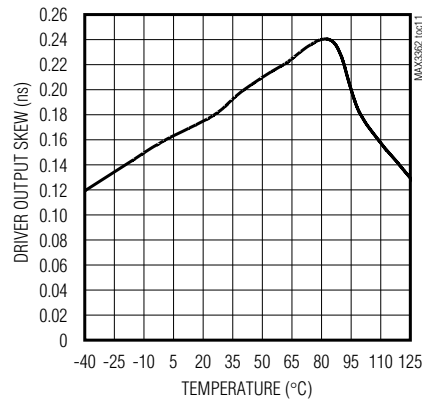
Typical Operating Characteristics (continued)

($V_{CC} = +3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)

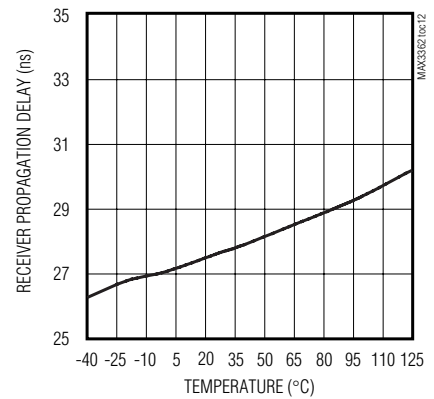
**SHUTDOWN SUPPLY CURRENT
vs. TEMPERATURE**



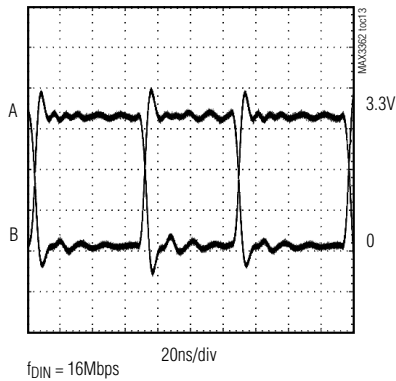
DRIVER OUTPUT SKEW vs. TEMPERATURE



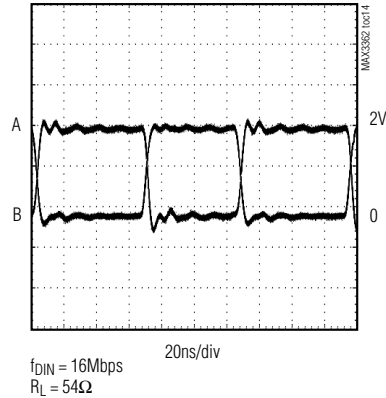
**RECEIVER PROPAGATION DELAY
vs. TEMPERATURE**



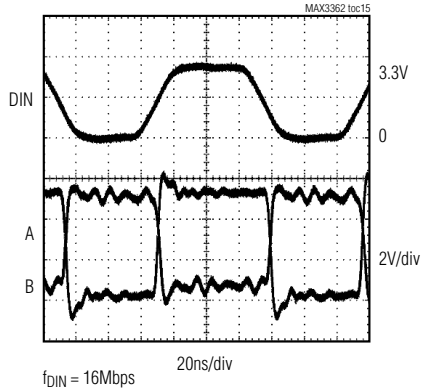
**UNLOADED DRIVER OUTPUT
WAVEFORM**



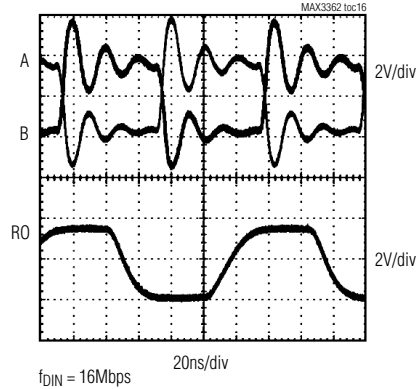
**LOADED DRIVER OUTPUT
WAVEFORM**



DRIVER PROPAGATION DELAY



RECEIVER PROPAGATION DELAY



3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

Pin Description

| PIN | NAME | DESCRIPTION |
|-----|------------------------|---|
| 1 | RO | Receiver Output. RO is high if the receiver input differential (A-B) $\geq 200\text{mV}$ and the receiver is enabled ($\overline{\text{RE}}$ is low). RO is low if the receiver input differential (A-B) $\leq -200\text{mV}$ and the receiver is enabled. |
| 2 | $\overline{\text{RE}}$ | Receiver Output Enable. Driving $\overline{\text{RE}}$ low enables RO. RO is high impedance when $\overline{\text{RE}}$ is high. Drive $\overline{\text{RE}}$ high and DE low (disable both receiver and driver outputs) to enter low-power shutdown mode. |
| 3 | DE | Driver Output Enable. Driving DE high enables driver outputs. These outputs are high impedance when DE is low. Drive $\overline{\text{RE}}$ high and DE low (disable both receiver and driver outputs) to enter low-power shutdown mode. |
| 4 | DI | Driver Input. Driving DI low forces the noninverting output low and inverting output high, when the driver is enabled (DE is high). Driving DI high forces the noninverting output high and inverting output low. |
| 5 | GND | Ground |
| 6 | A | Noninverting Receiver Input and Noninverting Driver Output |
| 7 | B | Inverting Receiver Input and Inverting Driver Output |
| 8 | VCC | Supply Voltage. VCC = 3.3V $\pm 5\%$. Bypass VCC to GND with a 0.1 μF capacitor. |

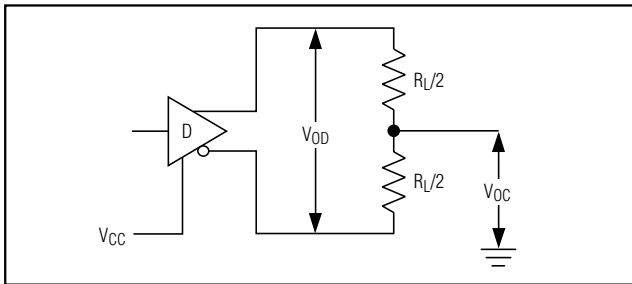


Figure 1. Driver DC Test Load

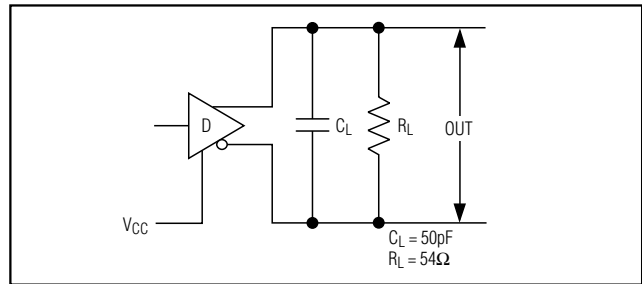


Figure 2. Driver Timing Test Circuit

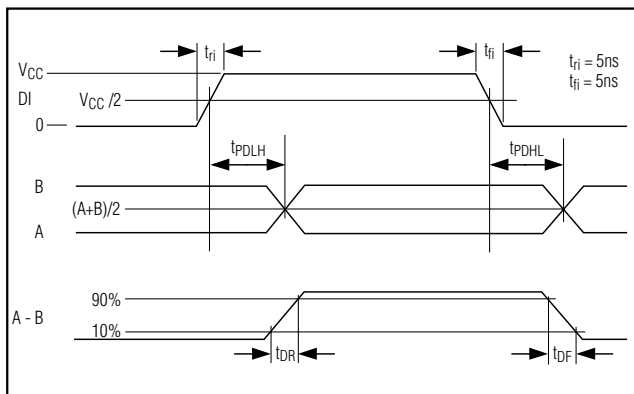


Figure 3. Driver Propagation Delay

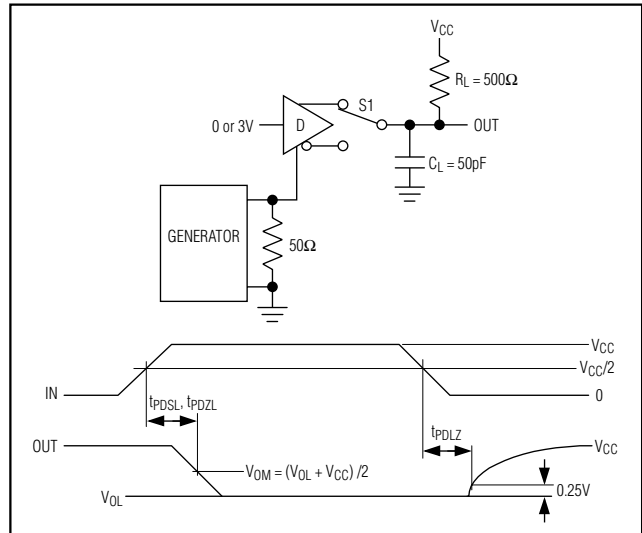


Figure 4. Driver Enable and Disable Times (t_{PDSL} , t_{PDZL} , t_{PDSL} , t_{PDLZ})

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

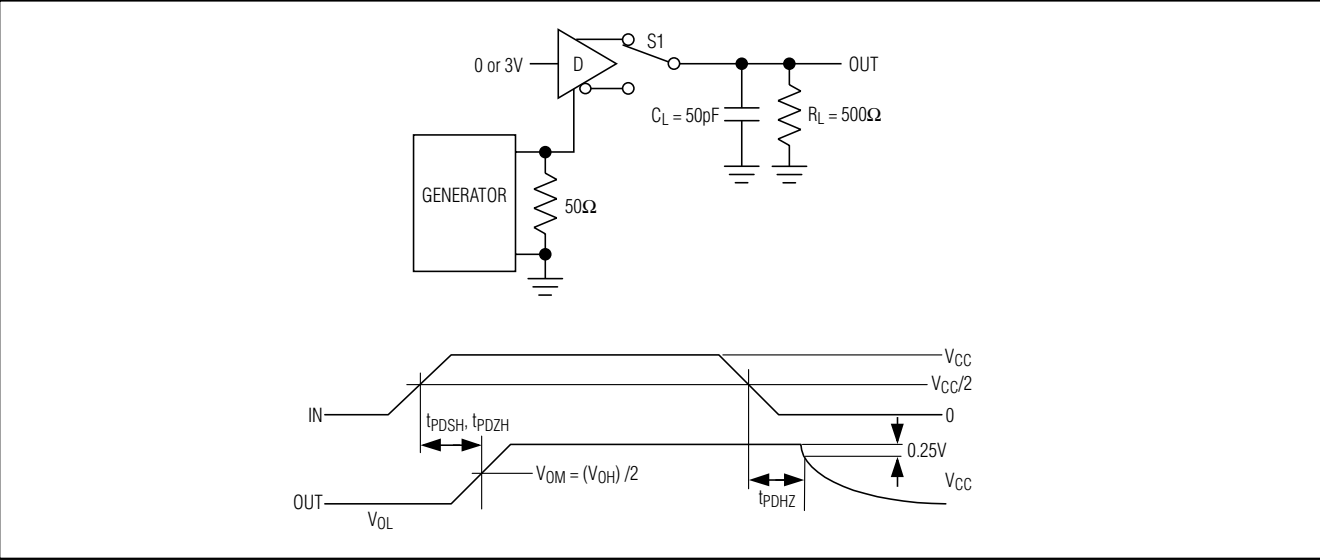


Figure 5. Driver Enable and Disable Times (t_{PDSH} , t_{PDZH} , t_{PDHS} , t_{PDHZ})

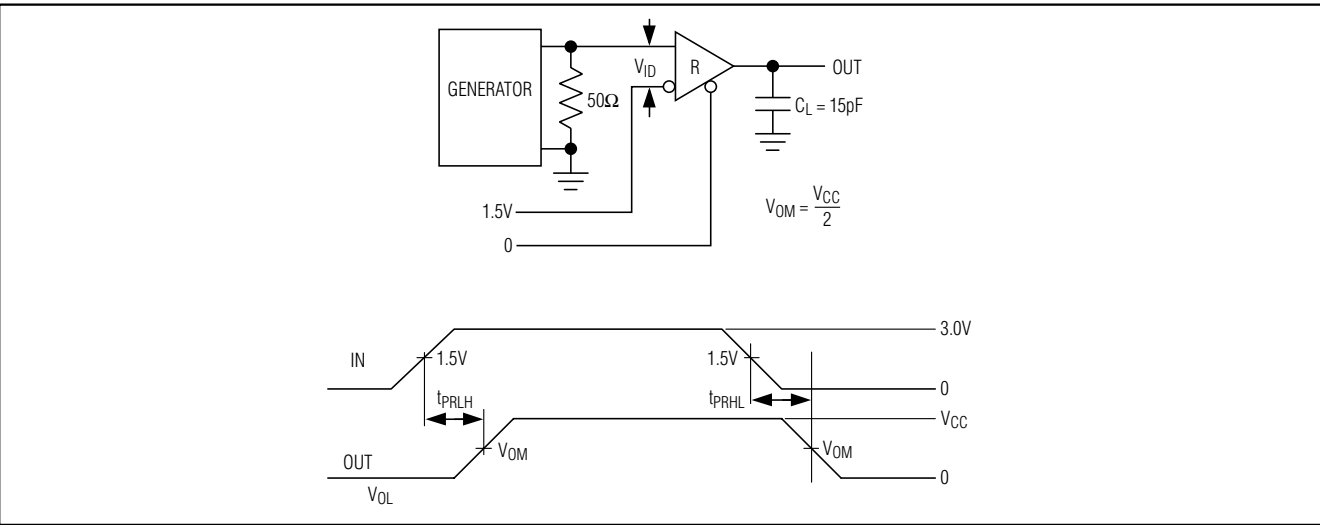


Figure 6. Receiver Propagation Delays

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

MAX3362

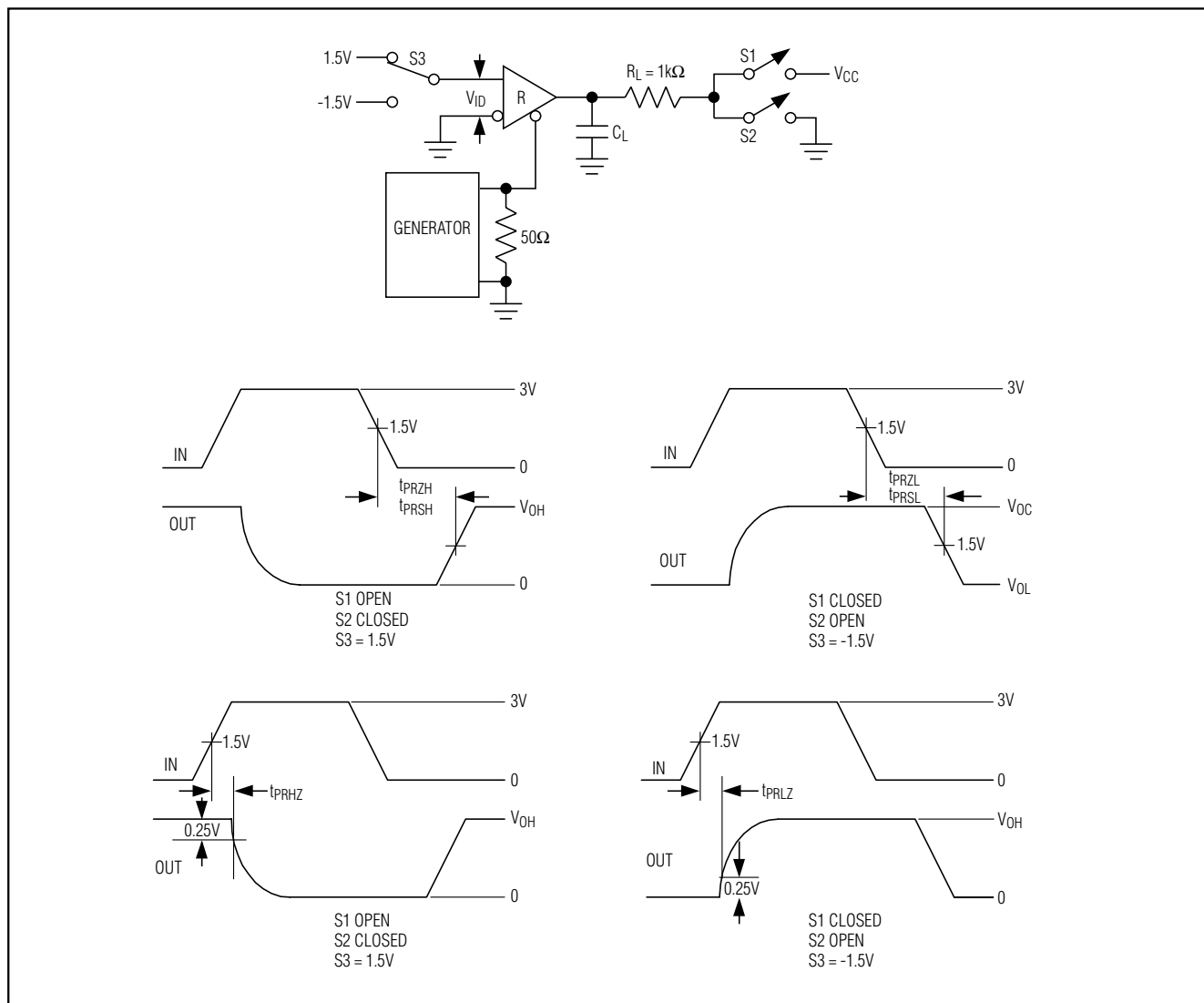


Figure 7. Receiver Enable and Disable Times

Detailed Description

The MAX3362 low-power, high-speed transceiver for RS-485/RS-422 communication operates from a single +3.3V power supply. The device contains one differential line driver and one differential line receiver. The driver and receiver may be independently enabled. When disabled, outputs enter a high-impedance state.

The transceiver guarantees data rates up to 20Mbps, with an output skew of less than 6ns. This low skew time makes the MAX3362 ideal for multidrop clock/data

distribution applications, such as cellular base stations. Driver and receiver propagation delays are below 50ns. The output level is guaranteed at 1.5V on a standard 54Ω load.

The device has a hot-swap feature that eliminates false transitions on the data cable during circuit initialization. Also, drivers are short-circuit current limited and are protected against excessive power dissipation by thermal shutdown circuitry.

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

Table 1. Transmitter Functional Table

| TRANSMITTING | | | | |
|------------------------|----|----|----------|--------|
| INPUTS | | | OUTPUTS | |
| $\overline{\text{RE}}$ | DE | DI | A | B |
| X | 1 | 1 | 1 | 0 |
| X | 1 | 0 | 0 | 1 |
| 0 | 0 | X | High Z | High Z |
| 1 | 0 | X | Shutdown | |

Table 2. Receiver Functional Table

| RECEIVING | | | |
|------------------------|----|----------------------|----------|
| INPUTS | | | OUTPUT |
| $\overline{\text{RE}}$ | DE | A – B | RO |
| 0 | X | $\geq 200\text{mV}$ | 1 |
| 0 | X | $\leq -200\text{mV}$ | 0 |
| 1 | 1 | X | High-Z |
| 1 | 0 | X | Shutdown |

The MAX3362 has a 1/8-unit-load receiver input impedance, allowing up to 256 transceivers to be connected simultaneously on a bus. The MAX3362 is designed for half-duplex communication.

Driver

The driver transfers single-ended input (DI) to differential outputs (A, B). The driver enable (DE) input controls the driver. When DE is high, driver outputs are enabled. These outputs are high impedance when DE is low.

When the driver is enabled, setting DI low forces the noninverting output (A) low and inverting output (B) high. Conversely, drive DI high to force noninverting output high and inverting output low (Table 1).

Drive $\overline{\text{RE}}$ high and DE low (disable both receiver and driver outputs) to enter low-power shutdown mode.

Receiver

The receiver reads differential inputs from the bus lines (A, B) and transfers this data as a single-ended output (RO). The receiver enable ($\overline{\text{RE}}$) input controls the receiver. Drive $\overline{\text{RE}}$ low to enable the receiver. Driving $\overline{\text{RE}}$ high places RO into a high-impedance state.

When the receiver is enabled, RO is high if (A-B) $\geq 200\text{mV}$. RO is low if (A-B) $\leq -200\text{mV}$.

Drive $\overline{\text{RE}}$ high and DE low (disable both receiver and driver outputs) to enter low-power shutdown mode.

Hot-Swap Capability

Hot-Swap Input

When circuit boards are inserted into a hot or powered backplane, disturbances to the enable and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the output drivers are high impedance and are unable to drive the DE input of the MAX3362 to a defined logic level. Leakage currents up to $10\mu\text{A}$ from the high-impedance output could cause DE to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE. These factors could improperly enable the driver.

When V_{CC} rises, an internal pulldown circuit holds DE low for at least $10\mu\text{s}$ and until the current into DE exceeds $200\mu\text{A}$. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

The MAX3362 enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 8). When V_{CC} ramps from 0, an internal $10\mu\text{s}$ timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a $300\mu\text{A}$ current sink, and M1, a $30\mu\text{A}$ current sink, pull DE to GND through an $8\text{k}\Omega$ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that may drive DE high. After $10\mu\text{s}$, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that may drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{\text{RE}}$ there is a complimentary circuit employing two PMOS devices pulling $\overline{\text{RE}}$ to V_{CC} .

Hot-Swap Line Transient

The circuit of Figure 9 shows a typical offset termination used to guarantee a greater than 200mV offset when a line is not driven (the 50pF represents the minimum parasitic capacitance that would exist in a typical application). During a hot-swap event when the driver is

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

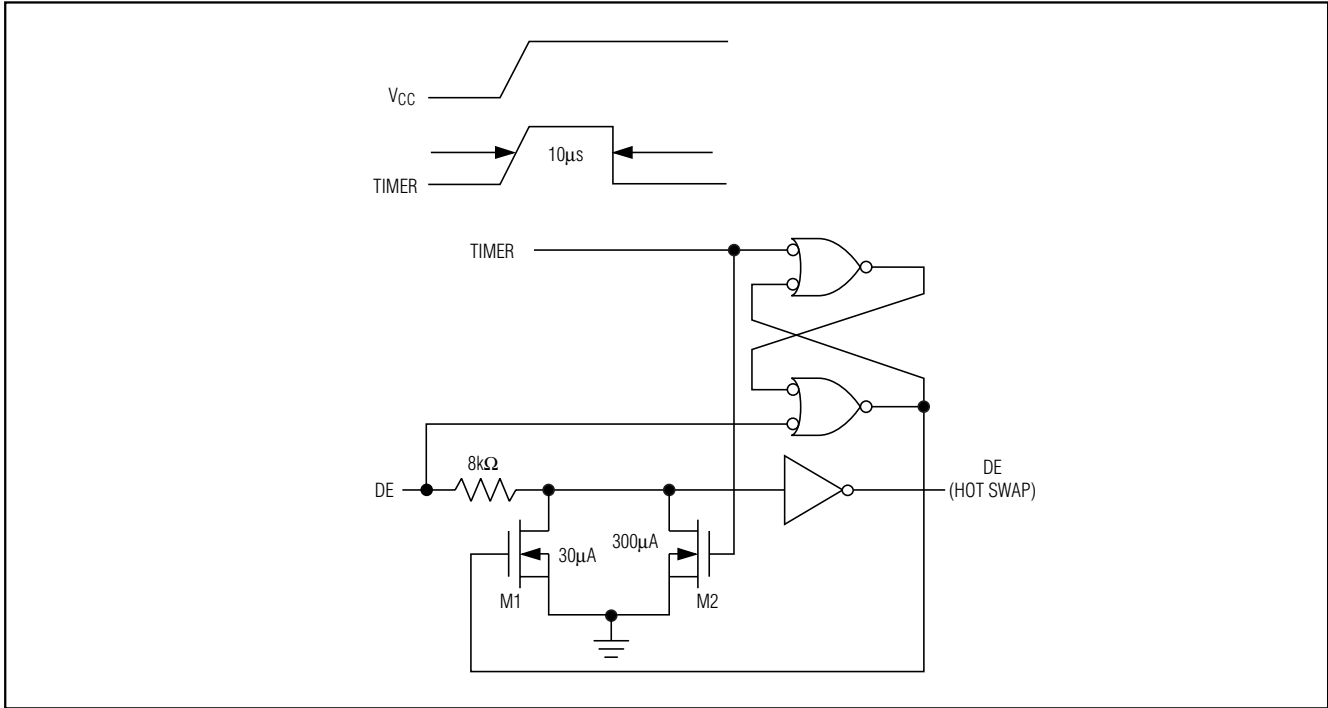


Figure 8. Simplified Structure of the Driver Enable Input (DE)

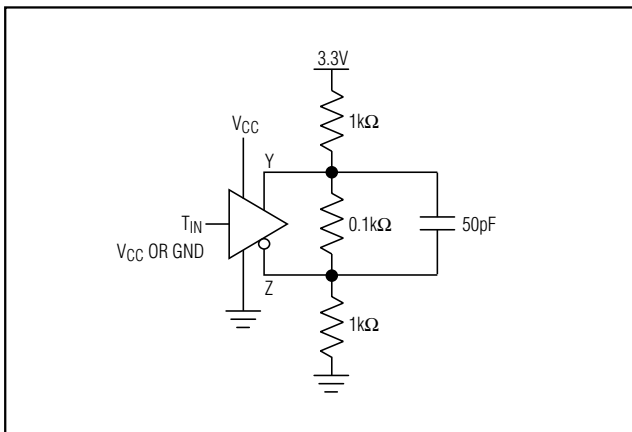


Figure 9. Differential Power-Up Glitch (Hot Swap)

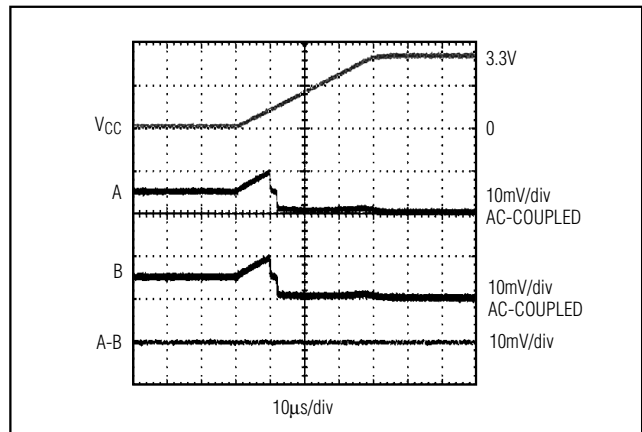


Figure 10. Differential Power-Up Glitch (0.1V/μs)

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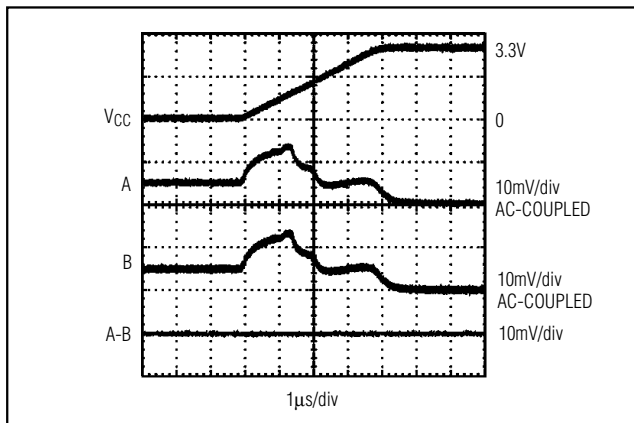


Figure 11. Differential Power-Up Glitch (1V/μs)

connected to the line and is powered up the driver must not cause the differential signal to drop below 200mV. Figures 10, 11, and 12 show the results of the MAX3362 during power-up for three different V_{CC} ramp rates (0.1V/μs, 1V/μs, and 10V/μs). The photos show the V_{CC} ramp, the single-ended signal on each side of the 100Ω termination, as well as the differential signal across the termination.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both \overline{RE} high and DE low. In shutdown, the MAX3362 typically draws only 1μA supply current.

\overline{RE} and DE may be driven simultaneously; the device is guaranteed not to enter shutdown if \overline{RE} is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the device will enter shutdown.

Enable times t_{PDZH} , t_{PDZL} , t_{PRZH} and t_{PRZL} in the *Switching Characteristics* table assume the device was not in a low-power shutdown state. Enable times t_{PDSH} , t_{PDSL} , t_{PRSH} , and t_{PRSL} assume the device was shut down. Drivers and receivers take longer to become enabled from low-power shutdown mode than from driver/receiver disable mode.

Applications Information

Propagation Delays

Figures 5 and 6 show the typical propagation delays. Skew time is simply the difference between the low-to-high and high-to-low propagation delay. Small driver/receiver skew times help maintain a symmetrical mark-space ratio (50% duty cycle). Both the receiver skew time and driver skew time are under 6ns.

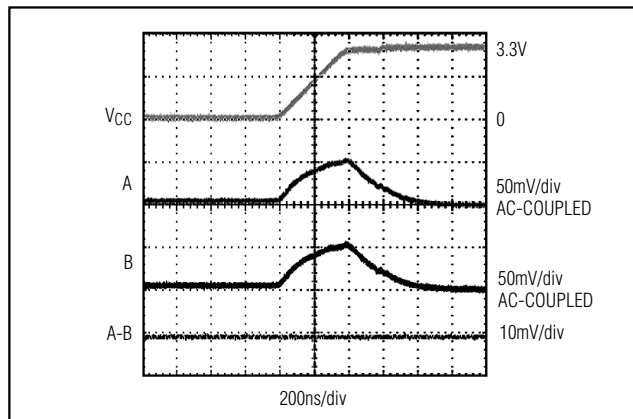


Figure 12. Differential Power-Up Glitch (10V/μs)

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (one-unit load), and a standard driver can drive up to 32 unit loads. The MAX3362 transceiver has a 1/8-unit-load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Driver Output Protection

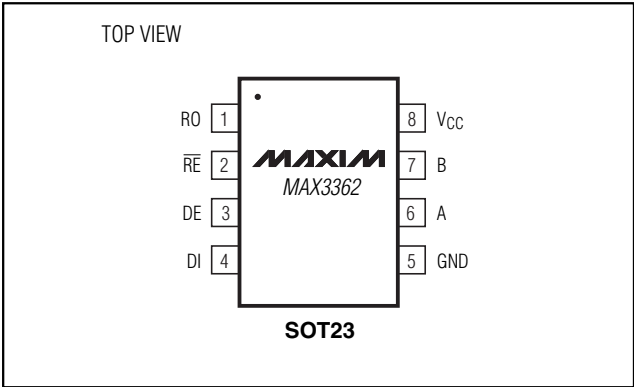
Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

Typical Applications

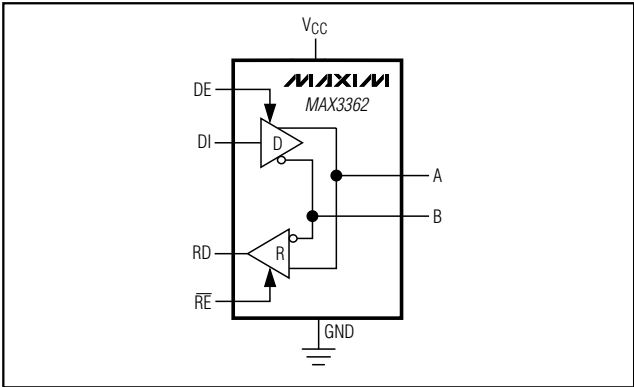
The MAX3362 transceiver is designed for bidirectional data communications on multipoint bus transmission lines. The *Typical Operating Circuit* shows a typical network applications circuit. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

Pin Configuration



Functional Diagram



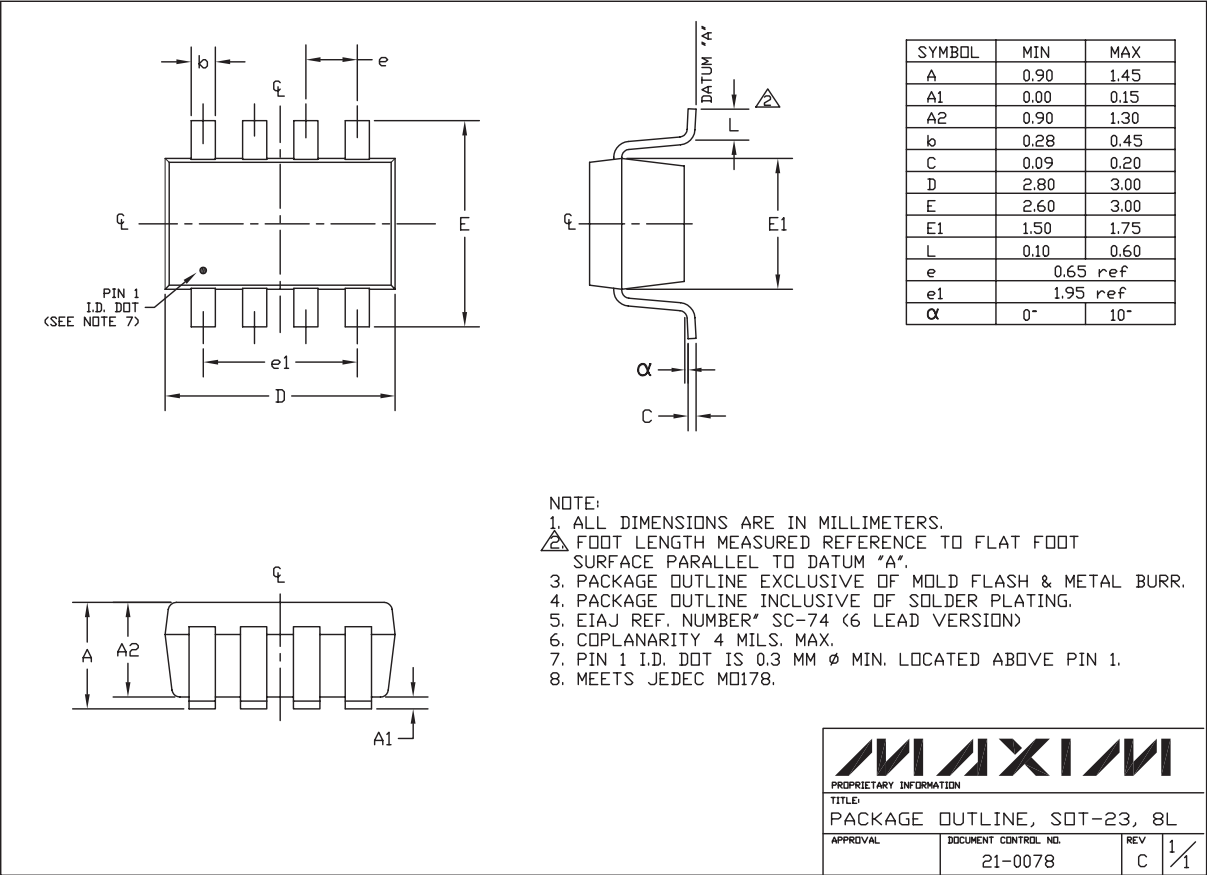
Chip Information

TRANSISTOR COUNT: 708
PROCESS: BiCMOS

3.3V, High-Speed, RS-485/RS-422 Transceiver in SOT Package

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



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